Application Note 1

Connecting the MT2xx0 Test System to Pentium®-based Boards (incl. DFT guidelines).

1. Introduction:

All members of the Pentium and Celeron family of processors are provided with debug 'hooks' or test points to enable hardware test and software debug. For the Pentium a 20 pin debug port is defined by Intel [1]; for the Pentium-Pro and beyond a 30 pin port is defined by Intel [2]. Using the debug header and the MT2xx0 the processor can be controlled by the user. Once in control, the processor can then be used as 'vehicle' for testing the entire motherboard.

Depending on the board design, there are various methods for connecting to the processor's debug 'hooks'. This application note describes the various methods, and suggests some DFT techniques for new designs which can simplify connection.

2. Designed-in Debug Port:

If a debug port is designed into the board as per the Intel specification [1] [2], then simply plug the MT2xx0 into this header.

3. Socketed Processor, Debug Port not Available:

If the processor is sockted or connected to a slot, International Test Technologies provide a range of interposers to aid connection. An interposer is a circuit board which sits between the processor and its socket or slot. A debug port is built into the interposer. To connect to a socketed processor just select the appropriate interposer from Table 1, fit it between the processor and socket, and plug the MT2xx0 into the interposer debug port.

Interposer For:	ITT Part No.
Pentium and Pentium MMX (293-pin PPGA/SPGA)	HW777-0121
Pentium-Pro	HW777-0211
Pentium II, Pentium III, Celeron (Slot 1)	HW444-0121
Pentium II Xeon, Pentium III Xeon (Slot 2)	HW444-0371
Pentium II Mobile MMC-1	HW777-0213
Pentium II Mobile MMC-2	HW777-0214
Celeron PPGA370	HW777-0215

Table 1: Interposer Types

4. Soldered-in Processor, Debug Port not Available:

If the processor is soldered-in and a designed-in debug port is not available, connection is still possible if certain signals are available. *These signals should be available at a suitable connector, or as simple test points. Some termination resistors may be required.* If the resistors are not already designed into the board, they should be fabricated into the MT2xx0 connecting cable.

Pin No.	Signal	Comments
1	INIT	
2	DBRESET	
3	RESET	CPU Reset. Use 33R resistor in series.
4	GND	At least one ground must be connected.
5	NC	
6	***Vcc***	3.3v. Connect 1K resistor in series.
7	R/S#	
8	GND	

9	NC	
10	GND	
11	PRDY	33R resistor in series.
12	TDI	
13	TDO	33R resistor in series.
14	TMS	
15	GND	
16	TCK	
17	GND	
18	TRST	
19	DBINST	
20	BSEN	
21-30	Not Used	

Table 2: MT2xx0 Pentium Processsor Probe Output Connector

This section describes the signals and terminations needed to implement a minimal debug port for the MT2xx0, for the various Pentium Processor types.

4.1 Pentium

The output of the MT2xx0 Pentium Probe is a 30-pin header. Only pins 1-20 of this header are currently used, as defined in Table 2. These pins correspond to Intel's 20-pin debug port definition [1]. Not all 20 signals are needed for successful MT2xx0 operation. Only the highlighted signals need to be included in your interface design. The termination resistors which should be built into the interface are specified in Table 2. Connection to the board can be via any suitable connector (Fig. 1), or by using spring-loaded test pins (Fig. 2).

4.2 Pentium-Pro:

The output of the MT2xx0 Pentium-Pro/Pentium II/III Probe is a 30-pin header. Only pins 1-20 of this header are currently used, as defined in Table 3. These pins correspond to Intel's 30-pin debug port definition [2]. Not all 30 signals are needed for successful MT2xx0 operation. Only the highlighted signals need to be included in your interface design. The termination resistors which should be built into the interface are specified in Table 3. Connection to the board can be via any suitable connector (Fig. 1), or by using spring-loaded test pins (Fig. 2).

4.3 Pentium II

As Pentium-Pro.

4.4 Pentium III

As Pentium-Pro.

4.5 Pentium II Xeon

As Pentium-Pro.

4.6 Pentium III Xeon

As Pentium-Pro.

4.7 Celeron

As Pentium-Pro.

Pin No.	Signal	Comments
1	RESET#	CPU Reset (GTL+ version)
2	GND	At least one ground must be connected.
3	DBRESET#	
4	GND	
5	TCK	150R Pull-up to Vcc (I/O)
6	GND	
7	TMS	150R Pull-up to Vcc (I/O)
8	TDI	150R Pull-up to Vcc (I/O)
9	POWERON	1K series resistor to Vtt or 1.5v
10	TDO	150R Pull-up to Vcc (I/O)
11	DBINST#	
12	TRST	
13	GND	
14	BSEN#	
15	GND	
16	PREQ0#	150R Pull-up to Vcc (I/O)
17	GND	
18	PRDY0#	
19	GND	
20	Not Used	
21-30	Not Used	

4.8 Connecting the Interface Cable to the UUT:

Once the interface cable is designed, connection to board can be made using a number of methods.

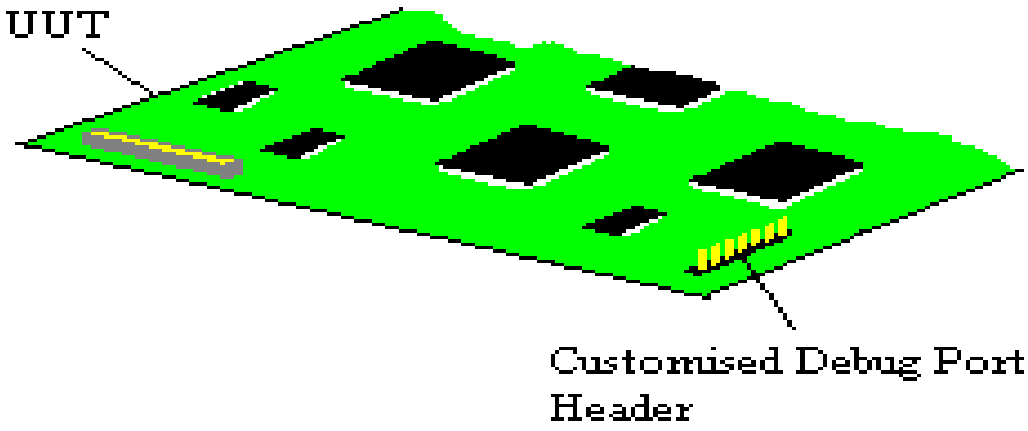
- Processor Module
 If the processor is mounted on a separate module, then mount a debug port header on a known-good pro cessor module. Use this 'gold' module for all testing (Fig.3).
- Test Header
 If the debug port signals are made available at a board connector or card edge, terminate the interface cable with the appropriate connector to mate with this test header (Fig. 1)
- Test Points
 If the debug port signals are available as a series of test points, a fixture will be required. The simplest form of fixture consists of a small sheet of perspex, with holes holding spring- loaded test pins at the test point positions, a debug port header, and mounting lugs to attach the fixture to the UUT (Fig. 2).

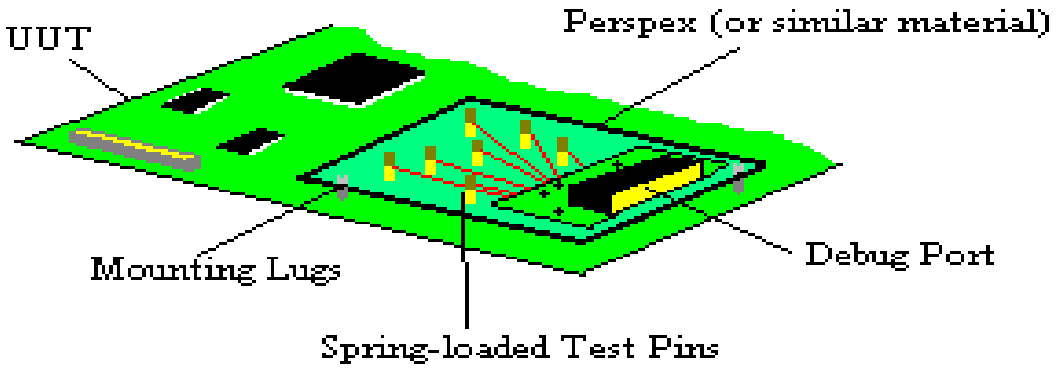
5. Some Considerations for Design for Test:

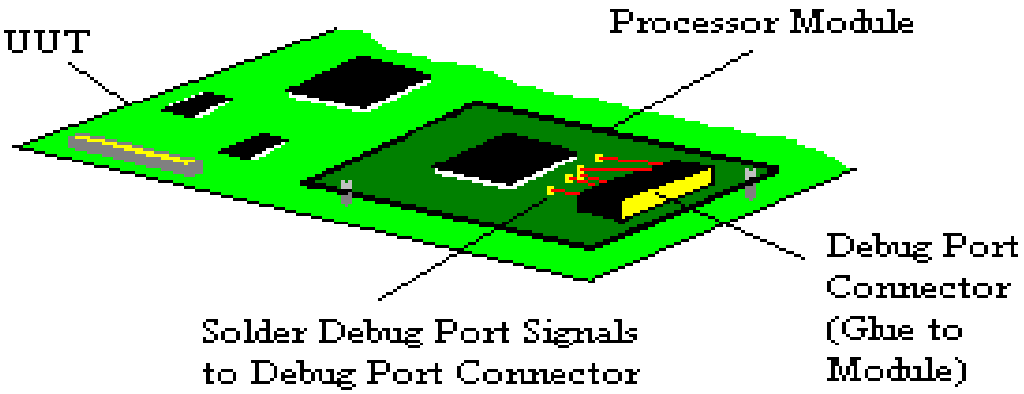
Refer to references [1] and [2]

A full debug port implementation is outlined in references [1] and [2]. A minimal debug port implementation can be constructed using only the signals specified in Table 2 and 3. The reduced number of signals should be made available at a suitable connecctor, or as test points (see Fig 1 and 2).

If the processor shares the boundary scan chain with other devices, a mechanism should be designed into the board to limit access to the chain, to debug port tools during testing. A full mechanism for doing this is described in [1] and [2].







Alternatively it can be achieved by just disabling TCK access to all devices except the processor; this can be implemented using gates or links.

6. Other Considerations:

6.1 Multiple Processors:

The MT2xx0 is a board tester, so only one processor is needed to facilitate board test. Use the master processor. The slave processor sockets/slots should be empty. However, if the UUT is based on a Pentium II Xeon or Pentium III Xeon, each slave slot should be populated with a terminator card.

6.2 System Reset

The MT2xx0 provides an OPTIONAL system reset probe via the trailing red and black wires which are part of the logic probe assembly. To enable an automated system reset, connect the red probe to the system reset. The black probe connects to ground.

The red probe connects to one of the following board positions:

- Across the reset switch
- Across the RC circuit used to generate the reset

- To the master reset input of a power monitor IC.
- To the power supply's power good signal

NB: If connecting via a UUT's own built-in debug port, do not connect this probe, as a built-in debug port has an embedded reset signal.

7. References:

[1] Pentium Processors Developer's Manual 1997. Available at http://developer.intel.com/design/mmx/manuals/

[2] P6 Family of Processors hardware Developer's Manual 1998. Available at http://developer.intel.com/design/pentiumII/manuals/

Note: As well as referring to the above manuals, it is also advisable to check the datasheet of the specific processor you are working with, for any variations in debug port design.

Further Information

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